

a fourth transistor for transferring said first voltage to said global word line according to potential of said node;

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder, wherein said local row decoder comprises:

a fifth transistor for transferring said global word line signal to said word line in response to a second signal;

a sixth transistor for transferring said global word line signal to said word line according to a third signal; and

a seventh transistor for transferring a ground voltage to said word line in response to said second signal.

6. (Canceled)

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7. (Currently Amended) The decoder circuit of claim <sup>5</sup>~~6~~, wherein said first and third transistors are consisted of PMOS transistor, and each of said second and fifth transistors ~~are~~ is consisted of an NMOS transistor.

8. (Canceled)

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9. (Currently Amended) The decoder circuit of claim <sup>7</sup>~~8~~, wherein said fifth transistor is consisted of a PMOS transistor, and each of said sixth and seventh transistors ~~are~~ is consisted of an NMOS